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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,577	12/03/2003	Sukeyuki Shinotsuka	7272-132/ 10314101	2295

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EXAMINER	
HSU, AMY R	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/729,577	SHINOTSUKA, SUKEYUKI	
	Examiner	Art Unit	
	Amy Hsu	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/3/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2-4, 8, 10-11, 15, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 2, it is unclear whether Claim 2 is dependent on Claim 1. Claim 2 uses Claim 1 for antecedent basis of "the first scanning means" and "the second scanning means", however claims limitations contradictory to Claim 1 and also contradictory to and having no support from the specification. According to the specification, specifically in Figures depicting the invention, Figs 7, 13, and 17, a Pixel Line Selecting Circuit is provided for sequentially selecting pixels on the line-by-line basis. This information from the specification is contradictory to Claim 2 which reads, "...the first scanning means comprises a pixel selecting circuit for providing signals for sequentially selecting pixels on the line-by-line basis..." It is indefinite whether Claim 2 intends to claim the first scanning means with a pixel *line* selecting circuit to select on a line-by-line basis, or whether Claim 2 intends to claim a first scanning means comprising a pixel selecting circuit to select on a *block-by-block* basis, as is consistent with Claim 1. Next, it is indefinite whether Claim 2 intends the second scanning means to select on a pixel-by-pixel basis as is consistent with Claim 1. There are at least two possible interpretations of Claim 2 in view of errors in the claim. In reference to Figure 7, if the first scanning means claimed in Claim 2 is reference number 1 and the second

is reference number 2, then the first scanning means should select on a line-by-line basis and the second scanning means should select on a block-by-block basis. In this case, Claim 2 should be changed to claim the first scanning means to comprise a pixel *line* selecting circuit, to indicate reference number 1. If this is the case, Claim 2 cannot be dependent on Claim 1 because Claim 1 claims the first scanning means selecting on a block-by-block basis and the second on a pixel-by-pixel basis, which is contradictory to Claim 1 in light of the definitions of block and line from the specification. However, if the first scanning means is reference number 2 and the second is reference number 7, as is consistent with Claim 1, then the first scanning means should select on a block-by-block basis, not line-by-line as Claim 2 reads, and the second should be on a pixel-by-pixel basis, not block-by-block as Claim 2 reads. If this is the case, Claim 2 can be dependent from Claim 1.

Regarding Claim 8, the same basis for rejection applies as for Claim 2, and Claims 3-4, 10-11, and 15 are dependent on the indefinite claims, which renders said dependent claims indefinite.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 9,14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimata (US 5998778), in view of Hedges et al. (US 5999211), further in view of Nomura (US 5933189).

Regarding Claims 1, 9,14, and 19, Kimata teaches an image sensor and method of controlling an image sensor (*Fig. 1, which is an improvement over Fig. 10, a focal plane array also called an image sensor in Col 14 Lines56-57 and Col 1 Line8-10*) comprising a matrix of solid-state light sensor elements (*Col 5 Lines 51-52, and Col 17 Lines 36-40 indicates a MOS, or solid-state element, as the desirable type of element used in the focal plane array, or image sensor matrix*), each of which represents a unit pixel (*Kimata teaches the matrix with rows of photodetectors, which is called a pixel row in Col 5 Line 56, therefore a photodetector corresponds to a pixel)* and is capable of reading out in a time series sensor signals of respective pixels (*Col 5 Lines 56-58 and Fig. 3 shows the time series associated with reading the signals))* by sequentially selecting pixel lines one by one (*Col 5 Line 56 describes the pixel row selection circuit which selects pixel lines one by one*) and sequentially selecting sensor signals one by one in a selected pixel line (*Col 16 Lines 19-23). Kimata teaches a first scanning means for seq*uentially reading out pixel sensor signals by selecting one line at a time (*one horizontal line, or pixel line in the array is selected as described in Col 6 Lines 26-30*), a second scanning means is provided for sequentially reading out pixel sensor signals on a pixel-by-pixel basis from a horizontal line (*signal charges are read out from the photodetectors in one horizontal line as described in Col 5 Lines 58-60).* Kimata fails to teach each of the pixel lines is evenly divided into a plurality of blocks with each

block composed of a specified number of pixels. However, Hedges teaches a camera and method of controlling a camera and focuses on an optical line array sensor and specifically teaches that the length of the pixel line is divided in *n* number of groups with each group containing *m* pixels (*Col 8 Lines 54-55).* It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Kimata's teachings of a scanning means involving selecting an individual pixel line, or horizontal line, with the teachings of Hedges to break the horizontal line into a certain number of groups with a certain number of pixels in each group because it could optimize the storage and or handling of the data associated with each pixel and each line if the selected horizontal line is broken into smaller groups. Neither Kimata nor Hedges teaches a bias circuit for converting sensor signals to voltage values with a reference voltage. However, Nomura teaches a bias circuit and method of controlling a bias circuit for converting a pixel sensor signal scanned by the first scanning means into a voltage value by using a reference resistance (*Fig. 16 reference number 209*) with a bias voltage applied thereto (*Col 39 Lines 10-17, Col 40 Lines 4-17*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kimata's teaching by adding the well known circuitry taught by Nomura to convert a pixel signal to a voltage using a reference resistance with a bias voltage applied because after pixel signals are scanned, the signals must be converted to voltages for further processing and storage.

5. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimata (US 5998778), in view of Hedges et al. (US 5999211).

Regarding Claims 7 and 18, Kimata in view of Hedges teaches an image sensor and method of controlling an image sensor comprising a matrix of solid-state light sensor elements, each of which represents a unit pixel and is capable of reading out in a time series sensor signals of respective pixels by sequentially selecting pixel lines one by one and sequentially selecting sensor signals one by one in a selected pixel line, characterized in that each of the pixel lines is evenly divided into a plurality of blocks with each block composed of a specified number of pixels and a first scanning means is provided for sequentially reading out pixel sensor signals on a block-by-block basis starting from a first block (*as addressed in the paragraph addressing Claim 1)*, a buffer means is provided for temporally storing pixel sensor signals of a readout block (*Col 16 Lines 9-10 describes the photodetector as a buffer means for temporally storing pixel sensor signals read from the first scanning means using the pixel row selection circuit)* and a second scanning means is provided for sequentially reading out the pixel sensor signals temporally stored in the buffer means (*Col 16 Lines 10-14 describe the next step which is reading out the signals from the buffer means and transfers the signals to storage gates*). Kimata teaches the method above in reference to the apparatus taught in the disclosure, therefore the apparatus, the second scanning means, to achieve the method above is also taught.

6. Claims 5-6, 12-13, 16-17, and 21-22 are rejected under 35 U.S.C. 103(a) as being obvious over Kimata (US 5998778), in view of Hedges et al. (US 5999211), further in view of Nomura (US 5933189)in view of Shinotsuka (US 7176435).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding Claims 5, 12, 16, and 21, Kimata in view of Hedges in view of Nomura teaches an image sensor as defined in claims 1, 7, 14, and 18 but fails to teach the limitations of Claims 5, 12, 16, and 21. Shinotsuka teaches an image sensor characterized in that the solid-state light sensor element is a light sensor circuit which is capable of producing in a photoelectric converting element a sensor current proportional to the quantity of light falling thereon, converting the sensor current into a voltage signal by a transistor with a logarithmic output characteristic in a weak inverse state, and outputting a sensor signal corresponding to the voltage signal (*Col 2 Lines*

15-22). It would have been obvious at the time the invention was made to one of ordinary skill in the art to combine the teachings of Shinotsuka because a logarithmic output characteristic in a weak inverse state achieves high sensitivity in detecting a light signal.

Regarding Claims 6, 13, 17, and 22, Kimata in view of Hedges in view of Nomura in view of Shinotsuka teaches an image sensor as defined in claim 5, 12, 16, and 21. Shinotsuka further teaches the image sensor characterized in that the light sensor circuit is initialized before detecting light by removing an electric charge remaining in a parasitic capacitor of the photoelectric converting element by changing a drain voltage of a MOS type transistor having a logarithmic output characteristic in a weak inverse state lower than a normal working value (*Col 2 Lines 22-27*). It would have been obvious at the time the invention was made to one of ordinary skill in the art to combine the teachings of Shinotsuka because the above described teachings enables the light sensor circuit to immediately obtain a voltage signal corresponding to the quantity of light falling on it at the time even if a sensor current rapidly changed, so the light sensor circuit may not cause an afterglow of the pixel even wit ha small quantity of incident light.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 5-6, 12-13, 16-17, and 21-22 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 7176435 in view of Kimata in view of Hedges in view of Nomura.

Regarding Claims 5 and 6, Claim 1-3 of US 7176435 teaches an image sensor and method of controlling an image sensor characterized in that the solid-state light sensor element is a light sensor circuit which is capable of producing in a photoelectric converting element a sensor current proportional to the quantity of light falling thereon, converting the sensor current into a voltage signal by a transistor with a logarithmic output characteristic in a weak inverse state, and outputting a sensor signal corresponding to the voltage signal, and characterized in that the light sensor circuit is initialized before detecting light by removing an electric charge remaining in a parasitic capacitor of the photoelectric converting element by changing a drain voltage of a MOS type transistor having a logarithmic output characteristic in a weak inverse state lower than a normal working value, however fails to teach the limitations of Claim 1,7,14, and 18. Kimata modified by Hedges and Nomura teach the limitations of Claims 1,7,14, and 18 as described in the paragraph addressing Claim 1. It would have been obvious

to combine the teachings of Shinotsuka with the teachings of Kimata modified by Hedges and Nomura because a logarithmic output characteristic in a weak inverse state achieves high sensitivity in detecting a light signal and because the teachings of Shinotsuka enable the light sensor circuit to immediately obtain a voltage signal corresponding to the quantity of light falling on it at the time even if a sensor current rapidly changed, so the light sensor circuit may not cause an afterglow of the pixel even wit ha small quantity of incident light.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure including Morris et al. (US6665010), Yang et al. (US 6975355), Hattori et al. (US 7151566), Jung (US 6731266), Egawa et al. (US 6999120).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy Hsu whose telephone number is 571-270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2609

ah

KENT CHANG
PRIMARY EXAMINER